1. (Amended) A platform to support one or more semiconductor processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a plurality of supporting members disposed between the lower mainframe and the upper mainframe, wherein each supporting member comprises sand.

2. The platform of claim 1, wherein the upper mainframe further comprises a fastener structure positioned proximate each one of the recesses, wherein the fastener structure is configured to hold the semiconductor substrate processing cell.

3. The platform of claim 1, wherein the upper mainframe further comprises a rigidifying plate and a main base plate comprising the plurality of recesses, the rigidifying plate comprising at least one aperture and attached to the main base plate such that the at least one aperture is aligned with the recesses.

4. The platform of claim 1, wherein the semiconductor substrate processing cell is a process cell.

5. The platform of claim 1, wherein the semiconductor substrate processing cell is a metrology cell.

6. The platform of claim 1, wherein the semiconductor substrate processing cell is an SRD cell.

7. (Cancelled) The platform of claim 1, wherein the dampener system comprises a plurality of support members that extend between the lower mainframe and the upper mainframe.

8. (Amended) (Allowed) A platform to support one or more semiconductor processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a plurality of support members between the lower mainframe and the upper mainframe, wherein each support member comprises:

a hollow tubular member;

a piston slidably disposed within the hollow tubular member; and

a dampening element contained within the hollow tubular member, wherein the piston is biased against the dampening element.

9. (Allowed) The platform of claim 8, wherein the dampening element is sand.

10. (Allowed) The platform of claim 8, wherein the dampening element acts as a vibration dampener.

11. (Allowed) A platform to support a cell, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a cell; and

a dampener system connecting the lower mainframe to the upper mainframe, wherein the dampener system comprises a plurality of support members that extend between the lower mainframe and the upper mainframe, each support member comprises:

a hollow tubular member,

a piston slidably disposed within the hollow tubular member, and

a dampening element contained within the hollow tubular member, wherein the piston is biased against the dampening element.

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12. (Allowed) The platform of claim 11, wherein the upper mainframe further comprises a fastener structure positioned proximate each one of the recesses, wherein the fastener structure is configured to hold the cell.

13. (Allowed) The platform of claim 11, wherein the upper mainframe further comprises a rigidifying plate and a main base plate comprising the plurality of recesses, the rigidifying plate comprising at least one aperture and attached to the main base plate such that the at least one aperture is aligned with the recesses.

14. (Allowed) The platform of claim 11, wherein the cell is a process cell.

15. (Allowed) The platform of claim 11, wherein the cell is a metrology cell.

16. (Allowed) The platform of claim 11, wherein the cell is a SRD cell.

17. (Cancelled) A platform to support one or more semiconductor substrate processing cells, comprising:

a lower mainframe;

an upper mainframe including a plurality of recesses, each one of the plurality of recesses configured to receive a semiconductor substrate processing cell; and

a dampener means disposed between the lower mainframe to the upper mainframe to support the upper mainframe relative to the lower mainframe.

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18. (Amended) The platform of claim 20, wherein the upper mainframe further comprises a fastener means positioned proximate each one of the recesses, wherein the fastener means is configured to hold the semiconductor substrate processing cell.

19. (Amended) The platform of claim 20, wherein the upper mainframe further comprises a rigidifying plate and a main base plate comprising the plurality of recesses, the rigidifying plate comprising at least one aperture and attached to the main base plate such that the at least one aperture is aligned with the recesses.